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TITLE

METHOD OF FORMING SHALLOW TRENCH ISOLATION WITH CHAMFERED CORNERS

BACKGROUND OF THE INVENTION

5 Field of the Invention

The invention relates to a process of forming shallow trench isolation. More particularly, the present invention relates to a manufacturing method of forming shallow trench isolation with chamfered corners.

10 Description of the Related Art:

Recently, as the manufacturing techniques of semiconductor integrated circuits develop, the number of devices in a chip has increased. The size of the device also decreases as the degree of integration increases. The
15 line width used in manufacturing lines has decreased from sub-micron to quarter-micron, or even smaller. Regardless of the reduction of the size of the device, adequate insulation or isolation must be provided among individual devices in the chip so that good element characteristics can
20 be achieved. This technique is called device isolation technology. The main object is to form an isolation region, reducing the size of the isolation as much as possible while assuring good isolation effect to allow larger chip space for more devices.

25 Among different device isolation techniques, LOCOS and shallow trench isolation region manufacturing methods are the two most used methods. In particular, as the latter has

a small isolation region and can keep the substrate level after the process is finished, it is the semiconductor manufacturing method obtaining the most attention.

The conventional manufacturing method for a shallow trench isolation region comprises forming a dielectric layer to fill a trench on a substrate by chemical vapor deposition (CVD), and etching back the dielectric layer on the substrate to remove the redundant dielectric layer. However, as the density of the semiconductor integrated circuits increases and the size of the elements decreases, the above mentioned deposition experiences problems in step coverage and cannot completely fill the trench. This influences the isolation effect among elements.

As a result of filling the entire trench which has a high aspect ratio, recently, high-density plasma chemical vapor deposition (HDPCVD) is used to form a dielectric layer on the substrate instead of CVD. In HDPCVD, the dielectric layer is deposited using O_2 and SiH_4 gases.

Figs. 1A~ 1C show a conventional fabrication process of a shallow trench isolation. In Fig. 1A, a pad oxide layer 12 is deposited on a substrate 10 such as Si substrate, wherein the thickness of the pad oxide layer 12 is about 50~200Å. The pad oxide layer 12 is formed using thermal oxidation or CVD. Thereafter, a silicon nitride layer 14 is deposited on the pad oxide layer 12 using CVD, and the thickness of the silicon oxide layer 14 is 500~2000Å. A mask layer thereby consists of the pad oxide layer 12 and the silicon nitride layer 14. Next, a patterned photoresist layer 13 is defined on the silicon nitride layer 14 and the pad oxide layer 12 using photolithography and etching

techniques to expose a portion of the substrate 10 where the shallow trench isolation is formed.

Next, In Fig. 1B, the exposed portion of the substrate 10 is etched using the silicon nitride layer 14 and the pad oxide layer 12 as a mask to form a trench 15, and the depth of the trench 15 is about 3500~5000Å. Then, a thin liner layer 16 is formed on the sidewall of the trench 15 using thermal oxidation process, and the thickness of the liner layer 16 is 180Å.

As shown in Fig. 1C, in HDPCVD, a dielectric layer 18 is deposited and fills the trench 15, wherein O_2 and SiH_4 are reactants.

As shown in Fig. 2, due to the opening of the trench narrowing and/or the aspect ratio of the trench increasing, for example the opening width may be less than $0.11\mu m$ and/or the aspect ratio larger than 4, the dielectric layer 18 deposited on the silicon nitride layer 14 may cover the opening of the trench 15 in the HDPCVD process, such that the dielectric layer 18 cannot fill the trench 15 completely and a void 20 is formed in the trench, resulting in poor insulation quality of the shallow trench isolation region.

Because the properties of the dielectric layer 18 are similar to those of the pad oxide layer 12, when etchant is used to dip pad oxide layer 12, the shallow trench isolation region 26 is inevitably etched so that the corner 22 of the trench 20 is exposed and an indentation 30 is formed adjacent to the corner 22 of the trench 20.

Thus, when the gate oxide layer and gate conductive layer are formed later, the conductive layer deposited in the indentation 30 is not easily removed and a short circuit

between the adjacent transistors easily occurs. In addition, since the gate oxide layer at the corner 22 of the trench 20 is thinner than other places, a parasitic transistor is formed. When current goes through this
5 parasitic transistor, as the curvature radius of the corner 22 of the trench 20 is small, the electric fields concentrate and the Fowler-Nordheim current increases, hence the insulating property of the gate oxide layer of the corner 22 degrades, resulting in abnormal element
10 characteristics. For example, there may be a kink effect in I-V curvature of I_d and V_g , which generates a double hump.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a method of forming shallow trench isolation with
15 chamfered corners to promote isolation among elements and avoid voids by increasing the gap-filling ability of the shallow trench isolation with improved corner configuration when the dielectric layer is filled thereinto.

Moreover, the present invention provides a
20 manufacturing method, which avoids forming a trench isolation region of parasitic transistors at the corner of the trench.

Furthermore, the present invention provides a
25 manufacturing method of forming a trench isolation region, which avoids short circuit between adjacent transistors.

To achieve the above mentioned objects, the method of forming shallow trench isolation with chamfered corners according to the present invention includes the following steps. First, a pad insulating layer, a first mask layer,

and a second mask layer are sequentially formed on a substrate. The second mask layer, the first mask layer, and the pad insulating layer are patterned to form an opening exposing a portion of the substrate. Next, the substrate is
5 etched using the patterned second mask layer as a mask to form a trench therein. Next, part of the second mask layer is removed to expose the first mask layer adjacent to the trench and result in the second mask layer having a tapered profile. Finally, the second mask layer, the first mask
10 layer, the pad insulating layer, and the substrate are etched along the tapered profile of the second mask layer to chamfer corners of the trench.

One aspect of the invention, before the insulator layer is formed, further comprises forming a shield layer on the
15 surface of the substrate, the trench, and the chamfered corners.

In the present invention, after chamfering the corners of the trench, the method of forming shallow trench isolation with chamfered corners according to the present
20 invention further comprises the following steps. The second mask layer is completely removed. The first mask layer and the pad insulating layer are etched to remove a predetermined width thereof to expose a portion of the substrate adjacent to the trench. An insulator layer is
25 blanketly formed on the exposed surface of the substrate and the chamfered corners thereof to fill the trench. The first mask layer and the pad insulating layer are removed to form the trench isolation region.

Another aspect of the invention, before the insulator
30 layer is formed, further comprises forming a lining oxide

layer on the surface of the substrate, the trench, and the chamfered corners.

The present invention also provides another method of forming shallow trench isolation with chamfered corners, including the following steps. First, a pad insulating layer, a first mask layer, and a second mask layer are sequentially formed on a semiconductor substrate. Then, the second mask layer, the first mask layer, and the pad insulating layer are patterned to form an opening exposing a portion of the semiconductor substrate. Next, the semiconductor substrate is etched using the patterned second mask layer as a mask to form a trench therein. Next, part of the second mask layer is removed to expose the first mask layer adjacent to the trench and result in the second mask layer having a tapered profile. Next, the second mask layer, the first mask layer, the pad insulating layer, and the substrate are etched along the tapered profile of the second mask layer to chamfer corners of the trench. Furthermore, the second mask layer is completely removed. A shield layer is formed on the surface of the substrate, the trench, and the chamfered corners. An insulator layer is blanketly formed on the shield layer to fill the trench. Finally, the first mask layer and the pad insulating layer are removed to form the trench isolation region.

According to another aspect of the invention, the method of the present invention further comprises, after removing the second mask layer, etching the first mask layer and the pad insulating layer to remove a predetermined width thereof and expose a portion of the semiconductor substrate adjacent to the trench.

A detailed description is given in the following embodiments with reference to the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood
5 from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIGS. 1A to 1C show cross sections of the manufacturing process of the conventional shallow trench isolation region;

10 FIG. 2 is a schematic diagram showing voids formed by filling the conventional shallow trench isolation region using HDPCVD;

FIG. 3 is a schematic diagram showing the indentations formed by etching in the conventional manufacturing process
15 of the shallow trench isolation region;

FIGS. 4A to 4J are cross sections illustrating the manufacturing process of a shallow trench isolation region with chamfered corners in accordance with the present invention.

20 DETAILED DESCRIPTION OF THE INVENTION

FIGS. 4A to 4J are cross sections of the manufacturing process of a shallow trench isolation region with chamfered corners in accordance with the present invention.

First, referring to Fig. 4A, a semiconductor substrate
25 100, for example silicon substrate, is provided. Herein, use of the term substrate includes devices formed within a semiconductor wafer and the layers overlying the wafer. Next, a pad insulation layer 102, a first mask layer 104 and

a second mask layer 106 are formed sequentially on the surface of the semiconductor substrate 100. Preferably, the pad insulation layer 102 such as pad oxide layer with a thickness of 50Å to 200Å is formed using thermal oxidation at 850-950C°, APCVD, or LPCVD. The first mask layer 104 such as silicon nitride with a thickness of 1000Å to 2000Å is formed using LPCVD at 750-800C°, wherein SiCl_2H_2 and NH_3 are reactants. As well, the first mask layer 104 may also be silicon oxy-nitride formed by LPCVD, wherein SiH_4 , N_2O , and NH_3 are reactants.

Suitable material for the second mask layer 106 is silicide such as boro phosphor silicate glass (BPSG), phosphor silicate glass (PSG), boro silicate glass (BSG), and arsenic silicate glass (AsSG). Preferably, the second mask layer 106, of BSG with a thickness of 1000 to 4000Å is formed by LPCVD, wherein SiH_4 , BF_3 , and B_2H_6 are reactants.

Subsequently, a patterned photoresist (PR) layer (not shown in Fig.) is coated on the surface of the second mask layer 106, and photolithography performed to define the photoresist pattern required. Moreover, the second mask layer 106, the first mask layer 104, and the pad insulating layer 102 are etched anisotropically (for example reactive ion etching), with the patterned photoresist acting as a mask.

Furthermore, the patterned photoresist layer is used as a mask to anisotropically etch the second mask layer 106, the first mask layer 104, and the pad insulating layer 102, for example reactant ion etching, to transfer the pattern of the photoresist layer to the second mask layer 106, the first mask layer 104, and the pad insulating layer 102 to

form opening 103, such that the semiconductor substrate 100 in the opening 103 is exposed, and the size of the opening 103 is substantially that of the isolation region. Then, suitable solution or dry etching is performed to remove the photoresist layer.

Subsequently, referring to FIG. 4B, the patterned second mask layer 106 is used as a mask to anisotropically etch semiconductor substrate 100, for example reactant ion etching, and a trench 105 with a depth 120 of 1800Å to 2400Å is formed.

Subsequently, referring to FIG. 4C, a wet treatment is then performed. The wet treatment includes using etchant, such as a solution of ammonium hydrogen peroxide mixture (APM), to etch both sides of the second mask layer 106 adjacent to the opening 103. After etching, part of the second mask layer 106 adjacent to the opening 103 with a width between 150~250Å is removed and the second mask layer 106 with tapered profiles 108 adjacent to the opening 103 is formed. Preferably, the ratio of $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$:deionized water (DIW) is about 1:1:5 and the etching temperature is 60C° or higher.

Subsequently, referring to FIG. 4D, anisotropic etching, for example RIE, is performed along the tapered profiles 108 of the second mask layer 106 to remove part of the second mask layer 106, the first mask layer 104, the pad insulating layer 102, and the semiconductor substrate 100 around the trenches 105. Then, the corners 110 of the trench 105 are chamfered, and a Y-shaped trench 105a is further formed. The depth 120a (for example, between 2700~3600Å) of the Y-shaped trench 105a is deeper than that

of the original trench 105, and the aspect ratio of the Y-shaped trench is between 4~6.

Subsequently, referring to FIG. 4E, the second mask layer 106 is completely removed by appropriate etching, for example, wet treatment with buffered hydrofluoric acid as etchant to etch the second mask layer 106 composed of BSG. Next, wet treatment etches both sides of the first mask layer 104 and the pad insulating layer 102 adjacent to the trench 105a until a width between 50~300Å thereof is removed, as shown in FIG. 4F. Preferably, a hydrofluoric acid/ethylene glycol mix (HF/EG) etches the first mask layer 104 and the pad insulating layer 102.

Subsequently, referring to FIG. 4G, a thermal oxidation process is performed to grow a shield layer 116 such as a liner oxide layer with a thickness of 50Å to 350Å in the bottom, sidewall, and chamfered corners of the trench 105a and the surface 117 of the substrate 110.

Subsequently, referring to FIG. 4H, an insulator layer 118, such as a silicon dioxide layer, with a thickness of 3000~5000Å is formed on the shield layer 116 by HDPCVD using O₂ and SiH₄ as reactants with Ar sputtering. Finally, referring to FIG. 4I, chemical mechanical polishing removes uneven insulator layer 118 to cover the shield layer 116 and leave the insulator layer 118 inside the trench 105a. The first mask layer 104 and the pad insulating layer 102 are then removed using adequate liquid or etching to expose the element region, as shown in FIG. 4J. Accordingly, the shallow trench isolation region 150 of the present invention is achieved. Preferably, the first mask layer is removed by, for example, a hot phosphoric acid solution and the pad

insulating layer 102 is removed by, for example, a HF solution.

Compared to the prior art, the manufacturing method of forming shallow trench isolation with chamfered corners in the present invention has several advantages.

First, the present invention prevents void in the high aspect ratio shallow trench isolation region to promote the insulation quality thereof. Particularly, the method according the present invention can be used to fill the trench having aspect ratio exceeding 6 with insulator layer by HDPCVD.

Second, the corners of the trench in the present invention are already chamfered and thickness of the shield layer subsequently formed in this region is the same as in the other regions, thus no parasitic transistors will form and problems with the parasitic transistors will not occur, so the method in the present invention avoids short circuit between adjacent transistors.

Since the corner of the trench of the present invention is already chamfered, the conductive material subsequently formed in this region has no space blockage and is easily removed, thus preventing short circuit between the adjacent transistors. Therefore, the shallow trench isolation region of the invention has good electrical insulation.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore,

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the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.